

EAST Browser [1.9 (54) 7 and select] [US 4093277] [Tag: 51 Doc: 49/54] [Full] 1/13 [Total images: 13]

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Kojima et al. [49] Date of Patent: Jan. 9, 1990

[54] SEMICONDUCTOR MEMORY

[75] Inventors: Kazuhiko Kojima, Matsuyama Shiro, both of Ohtsuka-shi, Japan

[73] Assignee: Hitachi, Ltd., Tokyo, Japan

[\*] Notice: The portion of the term of this patent subsequent to Oct. 25, 1999 has been disclaimed.

[21] Appl. No.: 886,814

[22] Filed: Oct. 14, 1988

Related U.S. Application Data

[62] Division of Ser. No. 879,072, Jan. 24, 1984, Pat. No. 4,786,415

[52] Foreign Application Priority Data

Jan. 14, 1983 JPT ..... 60-187793

[51] Int. Cl. G11C 7/00

[52] U.S. Cl. 368/208, 368/205

[54] Field of Search 365/149, 100, 203, 205, 363/210

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H. Kawamura et al., "A 256 Kb CMOS Pseudo SRAM", 1984 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 276-277.

Primary Examiner—Joseph A. Popko  
Attorney, Agent or Firm—Antonelli, Terry & Wando

[57] ABSTRACT

A dynamic RAM is arranged such that a common data line in each of the non-selected rows of the divided memory array is connected to a pair of common source lines of a sense amplifier corresponding to the memory array concerned, whereby the potential of the common data line is set at a medium level which is substantially equal to the potential of the data lines by utilizing the medium potential of the pair of common source lines and a relatively large parasitic capacity drawn, thereby maintaining the data lines at the half-precharge level. The pair of common source lines are shared to each column during the non-select period of the memory array, so that the common source lines have a medium level which is substantially equal to the half-precharge level of the data lines.

20 Claims, 3 Drawing Sheets

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DB: USPAT.US:POPUS:EPQ:JPD:DERWENT:BM:108

Default operator: DR

☐ Details ☒ Highlight all hit terms initially

(((common adj data adj line) and (read same control and write same control)) and sense) and during adj read and only) and coupled same common adj data

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef R
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20020048204 A1	20020425	49	Semiconductor integrated circuit device	365/200	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20010030889 A1	20011018	91	Nonvolatile semiconductor memory device	365/185.05	365/185.18; 365/185.29
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6438036 B2	20020820	92	Nonvolatile semiconductor memory device	365/185.22	365/185.18
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6407954 B2	20020618	17	Nonvolatile semiconductor memory device	365/201	365/189.05; 365/230.08
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6404694 B2	20020611	43	Semiconductor memory device with address comparing	365/230.03	365/189.01
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6259629 B1	20010710	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6181600 B1	20010130	94	Nonvolatile semiconductor memory device	365/185.18	365/185.22; 365/185.24
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6157576 A	20001205	94	Nonvolatile semiconductor memory device	365/185.29	365/185.21; 365/185.22
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6134169 A	20001017	15	Semiconductor memory device	365/222	365/189.04
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6064606 A	20000516	48	Semiconductor integrated circuit device	365/200	365/63
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6016273 A	20000118	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18

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	B	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef R
12	<input type="checkbox"/>	<input type="checkbox"/>	US 5991200 A	19991123	93	Nonvolatile semiconductor memory device	365/185.18	365/185.19; 365/185.22;
13	<input type="checkbox"/>	<input type="checkbox"/>	US 5959894 A	19990928	90	Nonvolatile semiconductor memory device	365/185.29	365/185.18; 365/185.22
14	<input type="checkbox"/>	<input type="checkbox"/>	US 5949715 A	19990907	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18; 365/185.24
15	<input type="checkbox"/>	<input type="checkbox"/>	US 5943278 A	19990824	10	SRAM with fast write capability	365/204	365/189.05; 365/189.11;
16	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5917752 A	19990629	92	Nonvolatile semiconductor memory device	365/185.18	365/185.22; 365/185.24
17	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5844842 A	19981201	93	Nonvolatile semiconductor memory device	365/185.24	365/185.29
18	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5818785 A	19981006	17	Semiconductor memory device having a plurality of banks	365/230.03	365/189.05; 365/230.06
19	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5781476 A	19980714	93	Nonvolatile semiconductor memory device	365/185.22	365/185.18; 365/185.19;
20	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5777921 A	19980707	26	Non-volatile semiconductor memory device	365/145	365/222
21	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5767544 A	19980616	47	Semiconductor integrated circuit device	257/318	365/200
22	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5615151 A	19970325	21	Semiconductor integrated circuit operable and	365/185.18	365/185.03; 365/185.06;

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 and sense) and during adj read and only) and coupled same common adj data

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	D	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
29	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5570241 A	19961029	15	Single channel, multiple head servo writing with	360/46	360/51; 360/68	
24	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5467314 A	19951114	8	Method of testing an address multiplexed dynamic RAM	365/201	365/193; 365/230.02	
25	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5457335 A	19951010	46	Floating gate FET with hydrogen barrier shield	257/318	257/630; 257/640;	
26	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5444663 A	19950822	22	Semiconductor integrated circuit operable and	365/226	365/189.09	
27	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5422858 A	19950606		Semiconductor integrated circuit	365/233	365/220; 365/239	
28	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5398047 A	19950314		Semiconductor integrated circuit device including	345/519	345/530; 365/230.05	
29	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5331596 A	19940719		Address multiplexed dynamic RAM having a test mode	365/201	365/193; 365/230.02;	
30	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5117393 A	19920526		Method of testing memory cells in an address	365/201	365/193; 365/233;	
31	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5097446 A	19920317		Nonvolatile semiconductor memory device	365/185.12	365/185.11; 365/185.21;	
32	<input type="checkbox"/>	<input type="checkbox"/>	US 5065363 A	19911112	24	Semiconductor storage device	365/154	365/189.05	
33	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5020028 A	19910528	13	Four transistor static RAM cell	365/154	257/369; 257/903	

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CAST Browser: L4: (10) sense adj. am. | US 5623444 | Tag: S | Doc: 15/10 | Full: 1/26 | Total images: 26

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the bit line capacitance charging operation. A **write** buffer operation, i.e., causing the capacitance component on a bit line to temporarily hold write charge information (high-speed bit line capacitance charging operation), can be performed at a relatively slow rate similar to a normal data access with respect to a DRAM (Dynamic Access memory). For information write operation to a memory cell trans within a short period write operation is via the memory (EEPROM) (a of the second object).

Detailed Description Text - DETX (19):

FIG. 1 shows part of the arrangement of the EEPROM. An actual memory cell array includes many main/sub bit lines, word lines, selection gate lines, selection transistors, memory cell transistors, and the like. These memory cell transistors are arranged in the form of a matrix. Row and column decoder circuits (peripheral circuits) for specifying a predetermined memory cell in accordance with an external address input are connected to this memory cell matrix. A bit line precharge circuit and a sense amplifier for reading stored data from a specified memory cell transistor are connected to each of a

United States Patent (79) **5,623,444**  
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INVENTOR: **DAVID J. KATZ**  
Attorney: **DAVID J. KATZ**

ABSTRACT

A memory device, such as a DRAM, is disclosed. The device includes a memory cell array, a word line decoder, a bit line decoder, a sense amplifier, and a precharge circuit. The memory cell array is arranged in a matrix. The word line decoder is connected to the memory cell array and the bit line decoder is connected to the memory cell array. The sense amplifier is connected to the memory cell array and the precharge circuit is connected to the memory cell array.

FIG. 1 is a schematic diagram of a memory device. The device includes a memory cell array 10, a word line decoder 20, a bit line decoder 30, a sense amplifier 40, and a precharge circuit 50. The memory cell array 10 is arranged in a matrix. The word line decoder 20 is connected to the memory cell array 10 and the bit line decoder 30 is connected to the memory cell array 10. The sense amplifier 40 is connected to the memory cell array 10 and the precharge circuit 50 is connected to the memory cell array 10.

17 Claims, 13 Drawing Sheets

FIG. 1 is a schematic diagram of a memory device. The device includes a memory cell array 10, a word line decoder 20, a bit line decoder 30, a sense amplifier 40, and a precharge circuit 50. The memory cell array 10 is arranged in a matrix. The word line decoder 20 is connected to the memory cell array 10 and the bit line decoder 30 is connected to the memory cell array 10. The sense amplifier 40 is connected to the memory cell array 10 and the precharge circuit 50 is connected to the memory cell array 10.

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further comprises a shared p-sense amplifier, a shared n-sense amplifier, and a plurality of n-channel depletion transistors selectively coupling the plurality of pairs of digit lines to the shared p-sense amplifier and the n-sense amplifier.

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FIG. 4

FIG. 5

RELATED ART

FIG. 4

FIG. 5

FIG. 4 is a schematic diagram of a memory array 100. It shows a grid of memory cells 101 connected to word lines 140 and bit lines 142. A sense amplifier 102 is connected to the bit lines. The array is divided into two sections by a dashed line 144.

FIG. 5 is a schematic diagram of a memory array 100. It shows a grid of memory cells 101 connected to word lines 140 and bit lines 142. A sense amplifier 102 is connected to the bit lines. The array is divided into two sections by a dashed line 144. The diagram includes labels for various components: 100, 101, 102, 140, 142, 144, 146, 148, 150, 152, 154, 156, 158, 160, 162, 164, 166, 168, 170, 172, 174, 176, 178, 180, 182, 184, 186, 188, 190, 192, 194, 196, 198, 200, 202, 204, 206, 208, 210, 212, 214, 216, 218, 220, 222, 224, 226, 228, 230, 232, 234, 236, 238, 240, 242, 244, 246, 248, 250, 252, 254, 256, 258, 260, 262, 264, 266, 268, 270, 272, 274, 276, 278, 280, 282, 284, 286, 288, 290, 292, 294, 296, 298, 300, 302, 304, 306, 308, 310, 312, 314, 316, 318, 320, 322, 324, 326, 328, 330, 332, 334, 336, 338, 340, 342, 344, 346, 348, 350, 352, 354, 356, 358, 360, 362, 364, 366, 368, 370, 372, 374, 376, 378, 380, 382, 384, 386, 388, 390, 392, 394, 396, 398, 400, 402, 404, 406, 408, 410, 412, 414, 416, 418, 420, 422, 424, 426, 428, 430, 432, 434, 436, 438, 440, 442, 444, 446, 448, 450, 452, 454, 456, 458, 460, 462, 464, 466, 468, 470, 472, 474, 476, 478, 480, 482, 484, 486, 488, 490, 492, 494, 496, 498, 500, 502, 504, 506, 508, 510, 512, 514, 516, 518, 520, 522, 524, 526, 528, 530, 532, 534, 536, 538, 540, 542, 544, 546, 548, 550, 552, 554, 556, 558, 560, 562, 564, 566, 568, 570, 572, 574, 576, 578, 580, 582, 584, 586, 588, 590, 592, 594, 596, 598, 600, 602, 604, 606, 608, 610, 612, 614, 616, 618, 620, 622, 624, 626, 628, 630, 632, 634, 636, 638, 640, 642, 644, 646, 648, 650, 652, 654, 656, 658, 660, 662, 664, 666, 668, 670, 672, 674, 676, 678, 680, 682, 684, 686, 688, 690, 692, 694, 696, 698, 700, 702, 704, 706, 708, 710, 712, 714, 716, 718, 720, 722, 724, 726, 728, 730, 732, 734, 736, 738, 740, 742, 744, 746, 748, 750, 752, 754, 756, 758, 760, 762, 764, 766, 768, 770, 772, 774, 776, 778, 780, 782, 784, 786, 788, 790, 792, 794, 796, 798, 800, 802, 804, 806, 808, 810, 812, 814, 816, 818, 820, 822, 824, 826, 828, 830, 832, 834, 836, 838, 840, 842, 844, 846, 848, 850, 852, 854, 856, 858, 860, 862, 864, 866, 868, 870, 872, 874, 876, 878, 880, 882, 884, 886, 888, 890, 892, 894, 896, 898, 900, 902, 904, 906, 908, 910, 912, 914, 916, 918, 920, 922, 924, 926, 928, 930, 932, 934, 936, 938, 940, 942, 944, 946, 948, 950, 952, 954, 956, 958, 960, 962, 964, 966, 968, 970, 972, 974, 976, 978, 980, 982, 984, 986, 988, 990, 992, 994, 996, 998, 1000.

Detailed Description text - DETX (3):

In the most general sense, a memory circuit comprises memory cells which store data. Depending upon the type of memory, this data can be read, or read and written. That is, some memories are read-only while others allow data to be read, manipulated, and re-written. Because many types of memories store data as a charge on a capacitor, sense amplifiers are implemented to detect small charges and amplify the charge for further processing. FIG. 1 is a simplified block diagram of a memory array 100 having memory cells 101 connected to a sense amplifier 102. The sense amplifier can be used to sense a charge stored on the memory cells and the charge back to the memory.

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Kajigaya et al.

(42) Date of Patent: Oct. 25, 1988

## [54] SEMICONDUCTOR MEMORY

[75] Inventors: Kazuhiko Kajigaya; Katsuyuki Sato, both of Kadoma, Japan

[73] Assignee: Hitachi, Ltd., Tokyo, Japan

[71] Appl. No.: 878,072

[21] Filed: Jan. 14, 1986

[35] Foreign Applications Priority Data

Jan. 24, 1985 (JP) Japan ..... 60-177793

[11] Int. Cl. .... G11C 7/00

[12] U.S. Cl. .... 365/208, 365/205

[13] Field of Search .... 365/149, 203, 205, 206, 365/210

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Conference, Digest of Technical Papers, pp. 274-277.

Primary Examiner—Joseph A. Papp

Attorney, Agent, or Firm—Antonelli, Terry &amp; Wanda

## [57] ABSTRACT

A dynamic RAM is arranged such that a common data line in each of the non-selected ones of the divided memory arrays is connected to a pair of common source lines of a sense amplifier corresponding to the memory array concerned, whereby the potential of the common data line is set at a medium level which is substantially equal to the potential of the data lines by utilizing the medium potential of the pair of common source lines and a relatively large parasitic capacity thereof, thereby stabilizing the data lines at the half-precharge level of the data lines.

18 Claims, 5 Drawing Sheets

